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# FPGA based Optimized Reconfigurable 29 Tap Fir Filter Design using Factored Canonic Signed Digit Technique

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**Abstract:** This paper reveals design and realization of 28 order efficient Finite Impulse Response (FIR) with equiripple characteristics for digital audio signal processing .In this paper the factorized canonical signed digit (FCSD) representation have been used to express the filter coefficients which reduces the design complexity, delay and area of FIR filter. FCSD guarantees the optimality by replacing binary coefficients specified with add and shift operation. FIR filter has been designed on MATLAB using equiripple technique and further the filter is synthesized on XilinxISE9.2 for Spartan 3EXC3S500EFG320-4, VIRTEX2PXC2VP30FF1152-5 FPGA devices. .The FIR filter is simulated I/O of 16 and 32 bit precision on MATLAB platform and FPGA structure. The behavioral simulation is proposed in VHDL model. Using an equiripple method with fixed point data type offers reduction in cost and minimum power consumption.

**Keywords:** FIR, Equiripple, FCSD, Sparten3E XC3S500E, Virtex2P.

## I. INTRODUCTION

In signal processing FIR plays an important role in analog or digital communication systems. A digital system is that which filters discrete as well as the input signal .There are many Application fields of FIR filters are some of them are speech synthesis, digital audio, noise elimination, speech recognition, Telecommunication, and other signal processing areas. FIR filters having exactly linear phase transients of finite duration. They require high order to have higher performance level, and provide better delay performance. Depending on the filter specifications the digital filters are designed to transmit the amount of data within the desired frequency band according to the specifications of filter. The applications like portable digitized filter which requires higher data rate and low power consumption affects the performance of the system in terms of reliability in cost by reducing life time of batteries. This results challenging task for the requirement of power delay and improvement in the performance of area.

In this paper FIR filter is designed using of a technology realizing FCSD representation. The field programmable gate array (FPGA) made developments with higher integration levels, By the equiripple approach the pass band and stop band noise can be reduced, and shapes the spectrum signal according to the usage The complexity exists in the filter because of coefficient multiplication operation The complexity can be reduced by presenting the coefficients of filters in FCSD **(factorized canonical signed digit) format.** Factored canonical representation makes reduction in cost by signed number of non zero digit of least number. FCSD is the coefficient representation of permissible digital sets. The work refers in here gives the approaches of tap value selected for the representation of binary and the FCSD representation. The sampling rates are very high, and clock edges provides new sample input produces new sample output during the analog to digital transition performance.

This paper introduces fully parallel FCSD technique FIR filter with proper design and schematics. According to the key design of the reduction in multipliers using add and shift method are the basic blocks of the proposed digitized filter. Density is determined by the designing factor, and using FCSD multiplications are computed by minimum hardware requirements by using the help of a shift and add operation.

The digitized parallel adders implement the fundamental arithmetic units of the filter design with FIR filter using FCSD .To overcome the difficulties of speed and cost such an algorithm is required to reduce the no of adders in order to designed of a suitable structure.

The proposed design implementation on FPGA in a distributed arithmetic mode. In higher order filters sufficient scope observed for more work in complexity reduction in the implemented FPGA .realization The work shows the design and implementation of parallel distributed Algorithm for FIR filter. The implementation result on FPGA is analyzed in terms of speed and the utilization of areas. For high order filters, speed of fully

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parallel architecture equals 3 times faster than compared to conventional FIR filter .Audio signal processing in the proposed work aims to improve the signal quality in noisy environment. The spectral subtraction method is suitable for the audio noise. The principle behind the spectral subtraction is to estimate noise from the magnitude spectrum, then subtracted from the original signal when the phase remains the same in the spectrum .
Low pass method for audio signal processing introduces where spectrum divided into different bands for better effective noise reduction .The performance of fully parallel with suitable architecture in low pass FIR filter is needed to support an order of 28 , and also to meet hardware requirements of VHDL .Since the analysis fully based on the filter builder of MATLAB supported by algorithms. The proposed work concluded that the symmetric structure of equiripple algorithm is the best solution for optimality. A filter having suitable architecture of order 28 which is necessary to fulfill hardware requirements, simulation, synthesis using VHDL. And VHDL designs are analyzed using different platforms like spartan3E, Virtex2P.

The rest of the paper is organized as follows: In Section I FIR filter overview and FCSD is covered in section II, section III includes FIR filter design on MATLAB, section IV comprises of hardware implementation, In section V Results and comparison, section VI concludes the complete paper.

1. FIR FILTER

Convolution operation performed in a digital filter having finit impulse response is called FIR filter. And also named as non recursive filter because of is not having any feedback. The equation is given by:

$$Y[n] = X[n]*H[n]$$

And the output can be described as

$$Y[n] = \sum_{k=o}^{N-1} H_k \, x\,(n-k)$$

Where $H_k$ and N be the coefficient and length of FIR filter. Generally FIR system consists of two structures, Transpose form and Direct form. Besides this Direct form 1 is used for the design of the low pass filter. In this the product of filter coefficient and sampled signals and are combined together in an adder block. The realization of direct form FIR filter is called tapped – delay-line or transversal filters. For symmetry conditions the linear phase FIR system with the unit sample response satisfies the equation given below:

$$h[n] = \pm\, h\,(M-1-n)$$

Fig I: below shows the general diagram of FIR filter for direct form I structure.

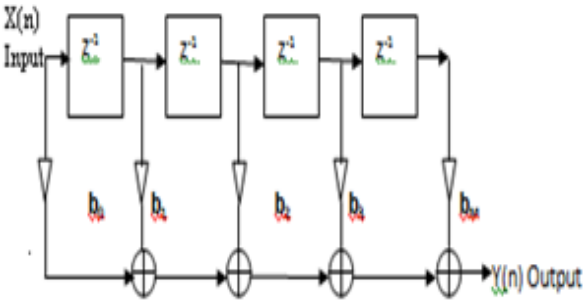


Figure1 .The general FIR filter for Direct form -I

The filter is designed by equiripple method. The low pass digital filter designed by calculating the filter coefficients according to the order of filter, sampling frequency stop band frequency , pass band frequency, stop band attenuation etc. In general the computation amount and the power consumption proportional directly to the order of the filter. Filter coefficient can be fixed by using MATLAB.

The coefficients of the proposed filter are symmetric in nature .Which results in reduced power consumption and area. N is the filter order and N+1 is the word length which is equal to the number of coefficients .The rate of system complexity and the amount delay time corresponds to the filter order.

## II. FACTORED CANONIC SIGN DIGIT ALGORITHM (FCSD)

In a digital FIR filter structure the canonic form means the transfer functions order equals to the number of delays in the block representation. The choice of FCSD approach is always applied a trade- off between the fast convergence and the computational complexity. So an optimal technique is selected to achieve the desired performance. .A filter for audio application has been selected, designed, implemented on FPGA device..FCSD replaces the multiplier operations and using the add and shift operations. Using FDA tool The combined effect of CSD representation and the factorization of filter coefficients gives rise to a reduction of number of adder numbers further reduces the hardware cost. using FDA tool The usage of LUTs and embedded multipliers of target devices causes the effective utilization ,and enhances the speed and provide the efficient area but increase in delay. The problem of propagation delay can solve using barrel shifter and carry save adder. Fully parallel filters never share hardware on the basis of multiple clock cycles so higher grade of resources required.

The architecture of FCSD independent of the number of taps and are of non-zero digits in each tap which assigns arbitrarily. The aim of author was to improve the coefficient's precision and reduce the filter complexity

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without any change in the performance of filter. This results a high speed lowpass FCSD based FIR filters. Simply we can say that FCSD mainly a binary number which encoded with a less number of non-zero bits .

Example: y = 99*x
=(3*33)*x
= 011*100001 in binary form
. = (10-1)* (100001) in CSD

Cost of FCSD = 2 adders, If we are using CSD or other algorithms the number of adders increases.

## III. FIR FILTER DESIGN ON MATLAB

The key intension of the author to implement the filter design in hardware platform. The specifications of the FIR filter is

1. Defining specifications such as type, order, structure, pass band frequency, stop band frequency, attenuations.
2. Calculation of filter coefficient.
3. Application of FCSD algorithm among filter coefficient.
4. On target FPGA check the filter coefficients. Finally check the configured FPGA target SPARTAN 3eXC3S500E FG320-4 , VIRTEX2PXC2VP30F F1152-5 for real. .

Table 1 shows the specification parameters of the filter having 29 tap.

TABLE1. FIR filters design specifications.

| | |
|---|---|
| ORDER | 28 |
| STRUCTURE | DIRECT FORM 1 |
| RESPONSE | LOWPASS |
| DESIGN METHODS | EQUIRIPPLE |
| PASSBAND FREQUENCY | 4KHz |
| STOPBAND FREQUENCY | 7KHz |
| PASSBAND ATTENUATION | 1dB |
| STOPBAND ATTENUATION | 80dB |

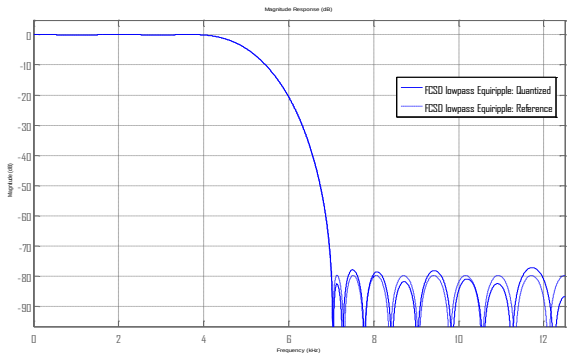


Fig 2 FCSD. Low pass Equiripple FIR filter magnitude response

Figure2 shows, the proposed FIR structure designed on MATLAB FDA Tool. The direct form symmetric structure gives the optimal result for cost effectiveness and area efficiency .The implementation automatically fully placed and routed with standard software on various devices of FPGA to realize the hardware preformancefor a maximum frequency and cost effective device utilization for audio signal processing.

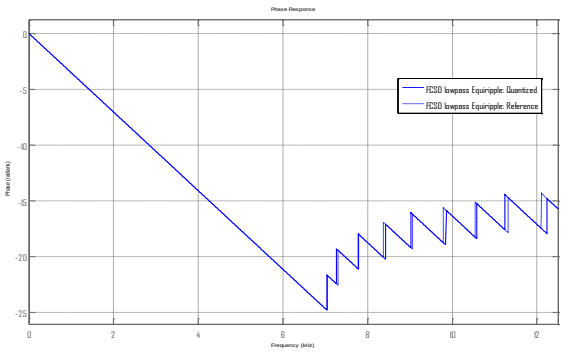


Fig 3. Phase response FCSD low pass Equiripple FIR filter.

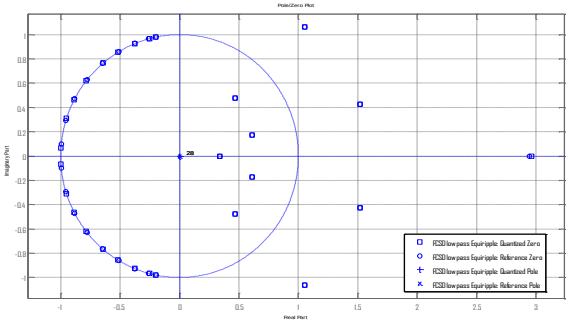


Fig 4 Pole-Zero plot FCSD low pass Equiripple FIR Filter.

## IV. HARDWARE IMPLEMENTATION

The proposed low pass FIR filter architecture implemented and described using VHDL synthesized on Xilinx ISE. exact measurements as well as the filter architecture are verified and tested by the behavioral modeling there are two parts to check first is the verification of state machine which goes through the exact states. The second one is to generate the correct output.

To attain the maximum frequency i.e., speed optimization at high grade the proposed FCSD based low pass FIR filter architecture intended to reduce the filter coefficient and thereby reducing the complexity of the structure of system without affecting the performance. For this a 29 tapped FIR filter architecture have been implemented in two different devices namely Spartan3E, Virtex2P,. The performance analysis on the basis of comparison with

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which device is suitable for the design aspects (. hardware resources and speed) And the output is plotted.

Fig 4. Below shows the design utilization implementation with direct symmetric FIR filter. Plots in the fig 4. based on data sampled with FPGA.

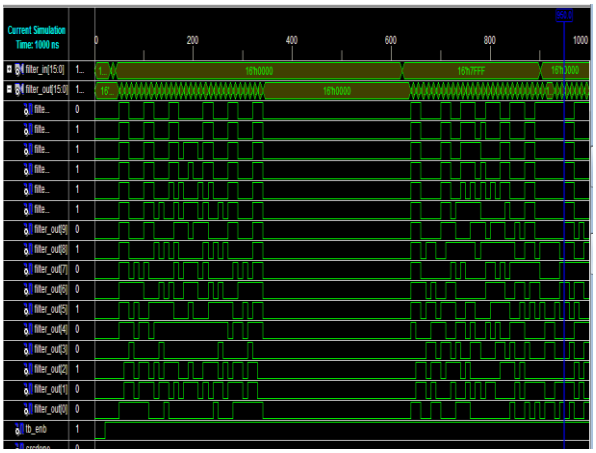

FIG 5 FIR FILTER SIMULATION OUTPUT

## V. RESULTS AND COMPARISON

The performance of two devices are obtained. The comparison made by According to the device utilization and maximum frequency produced.

Fig 6 Performance comparison of SPARTAN3E, VIRTEX2P

| Sl No | Logic utilization | SPARTAN3E | VIRTEX2P |
|---|---|---|---|
| 1 | Number of slices | 45% | 15% |
| 2 | Number of slice flip flop | 5% | 1% |
| 3 | Number of 4 input LUTs | 40 | 13% |
| 4 | Number of bonded IOBs | 15% | 5 |
| 5 | Number of GCLKs | 4% | 6% |

Fig7: Device utilization summery

| Sl no | Performance | **SPARTAN3E** | **VIRTEX2P** |
|---|---|---|---|
| 1 | Number of Slices | 2121 out of 4656 45% | 2121 out of 13696 15% |
| 2 | Number of Slice Flip Flops | 480 out of 9312 5% | 480 out of 27392 1% |
| 3 | Number of 4 input LUTs | 3743 out of 9312 40% | 3743 out 27392 13% |
| 4 | Number of bonded IOBs | 35out of 232 15% | 35 out of 644 5% |
| 5 | Number of GCLKs | 1 out of 24 4% | 1 out of 16 6% |

Fig 7. Shows the design summery of the two FPGA devices gives a clear cut in terms of device utilization spartan3E is better compared with virtex2P .In the proposed work29 tap low pass filter designed with the reduced hardware complexity with 80dB attenuation. From the timing comparison of two we can see that virtex 2P is better.

Fig 8 Timing Summary comparison:

| Sl no | Information | Implementation | |
|---|---|---|---|
| | Timing Summary: | **SPARTAN 3E** | **VIRTEX2P** |
| 1 | Minimum period | 79.706ns | 75.310ns |
| 2 | Maximum Frequency | 12.546MHz | 13.278MHz |
| 3 | Minimum input arrival time before clock | 3.177ns | 3.199ns |
| 4 | Maximum output required time after Clock | 4.283ns | 3.997ns |

Fig 8 shows the the comparison of timing summery between the two devices. Among them the maximum speed attained by Virtex2P.

Timing Summary: SPARTAN 3eXC3S500E FG320-4
---
Speed Grade: -4

Minimum period: 79.706ns (Maximum Frequency: 12.546MHz)
Minimum input arrival time before clock: 3.177ns
Maximum output required time after clock: 4.283ns
Maximum combinational path delay: No path found .

Timing Summary:, VIRTEX2PXC2VP30F F1152-5
---
Speed Grade: -5

Minimum period: 75.310ns (Maximum Frequency: 13.278MHz)
Minimum input arrival time before clock: 3.199ns
Maximum output required time after clock: 3.997ns
Maximum combinational path delay: No path found

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FIG. below shows bar graph containing design utilization in percent and speed in MHz Of the two devices in comparison mode.

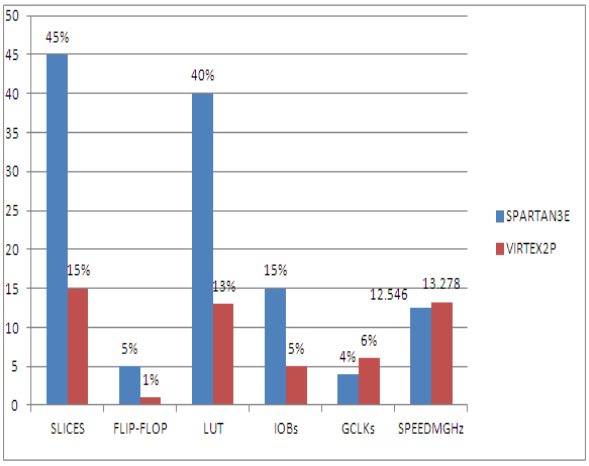


Fig 9: BAR GRAPH OF DESIGN UTILISATION AND SPEED.

## VI. CONCLUSION

This paper designs a29 tap optimal FIR filter using FCSD approach. The proposed optimal filter is designed add shift method and simulated on Spartan 3E, virtex2P, and basedXC3S500E FG320-4, XC2VP30 FF1152-5, and respectively. This concluded that by reduction in complexity and the maximum speed attained using each devices are 12.546MHz on spartan3E, 13.278MHz on virtex2P, The results obtained on FPGA device shows that filter designed on Spartan 3Eis producing best utilization factor as compared to virtex2P .In terms of speed filter designed on virtex2P is producing higher frequency as compared to Spartan3E .

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## BIOGRAPHY

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